A HIGH-PRECISION COUNTER USING THE DSP TECHNIQUE

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Abstract

A high-precision counter using a digital signal processor (DSP) is designed for phase and frequency measurement. We use an analog-to-digital converter (ADC) to sample the device under test (DUT). Once the signal is digitized, the DSP will be used to run the phase correlation and obtain the necessary information. In our design, the counter is implemented on the Texas Instrument (TI) TMS329C6201 digital signal processor. The sample data from the ADC are input to the DSP. Additionally, the 5 MHz frequency from the Telecommunication Laboratories (TL) standard is used as the reference of the synthesized signal generator. Then the synthesized signal generator produces the specific frequency in the ADC to serve as the reference clock. The ADC will then sample the signal of the DUT. The frequency difference between the signal and the specific frequency of the synthesized signal generator is approximately 1 Hz and the floating part of the frequency produced by the DUT. In the DSP, the phase correlation is created for finding the floating part of the frequency. The 1-second sampling data are correlated with the next second's. The result of the correlation operation can produce the phase shift in a 1-second interval. Finally, we can determine the frequency difference between the DUT and the reference clock of the ADC. The resolution of the frequency accuracy can be 5×10^{-12}.

INTRODUCTION

Because the stability of standard frequency sources, like cesium or rubidium clocks, is about 2×10^{-11} to 5×10^{-12} in a 1-second interval, a common counter cannot be used to measure their stability at intervals equal to or less than 1 second. For this reason, we design a high-precision counter for satisfactory performance with such clocks. In fact, a "software radio" is a good way to measure the frequency difference and phase difference of the device under test (DUT). The primary goal of a software radio is the minimal amount of hardware that is used in a radio. Conceptually, one can tune the radio through software or even change the function of the radio; therefore, great flexibility can be achieved. In general, the software radio uses an analog-to-digital converter (ADC) to sample the input signal, and the input signal is digitized as close to the antenna as possible. Once the signal is digitized, digital signal processing is used to obtain the necessary information. Additionally, a high-speed digital signal processor (DSP) works very well in a software radio. So the digital signal processing can be implemented by the DSP, for example, the filter, the Fast-Fourier transform, the phase-lock loop, etc. In general, the frequency outputs of the standard frequency source are 5 MHz and 10 MHz, and the frequency is in the baseband of the software radio. So we try to use the ADC to sample the frequency

source output.

The reference clock of the ADC can be the time reference of the sampling data. If the reference clock of the ADC is input by the primary frequency source, the frequency difference between the DUT and the frequency that approaches the DUT and equal to an integer times the primary frequency source will be the fundamental frequency in the sampling data. In our design, the fundamental frequency is about 1 Hz. In the DSP, the 1-second sampling data are correlated with next second's. The result of the correlation operation can produce the phase shift in a 1-second interval. Finally, we can determine the frequency difference between the DUT and the reference clock of the ADC.

Despite the fact that the ADC in our system runs at about 40 MS/s, the speed of the DSP is not good enough to process all the 1-second samples. The cache memory is also not sufficient to store all the sampling data. So we cut the data rate down to about 10 KS/s in the DSP. And the system resolution is designed to be 5×10^{-12}. This paper provides a brief introduction to the software radio in our system. Then it describes the system architecture. The system error in the system is considered. Finally, a self-test of our system is presented.

SYSTEM ARCHITECTURE

In our system, we use an ADC to sample the DUT. Once the signal is digitized, the DSP is used to run the phase correlation and obtain the necessary information. Figure 1 shows the block diagram of the system. In our design, the time base of the sampling data must be synchronized with the primary frequency standard. So the 5 MHz frequency from the Telecommunication Laboratories (TL) standard is used as the reference of the synthesized signal generator HP8662A. Then the synthesized signal generator HP8662A produces the specific frequency, 39,999,992 Hz in the ADC to serve as the reference clock. The maximum of the sampling rate is 39,999,992 S/s. Because the speed of the DSP is not good enough to process all the 1-second samples, we divide the sampling rate by 4,000 in the DSP. So the sampling rate is 9,999.998 S/s.

The frequency difference between the signal and the specific frequency of the synthesized signal generator is approximately an integer times the sampling rate of 1 Hz and a floating part of the frequency produced by the DUT. Because the frequency difference is related to the DUT frequency accuracy, the DUT frequency accuracy can be calculated from the number of sampling data in a cycle of the difference frequency. Figure 2 shows the relation between the DUT frequency accuracy and the number of the sampling data in a cycle of the difference frequency.

In general, the integer part of the sampling number in a cycle is not good enough to achieve an accuracy less than 2×10^{-11}. For this reason, a correlation operation is performed for calculating the floating part of the sampling number. The 1-second sampling data are correlated with the next second's, and the correlation discriminate is designed to search the peak of the integer correlation result. The three points that are approaching the peak are used to make the quadratic fit, and the maximum correlation result can be obtained. We can use it to determine the floating part of the sampling number. Figures 3 and 4 show the correlation operation and the floating part determined by the quadratic fit. Finally, the number of sampling data in a cycle of the difference frequency can be mapped to the DUT frequency accuracy. It is shown in Figure 5.

SYSTEM ERROR

The system contains some errors, and the errors will influence the measurement resolution. The errors are the quantization error, the ADC sampling noise, and the ADC time base error. Because the ADC resolution is 8-bit, the ADC that converts the analog signal to digital data will cause an accuracy error of about 5×10^{-12} in the system. The ADC sampling noise relative to the system is small. In fact, the quantization error and the ADC sampling noise will be reduced when the number of the sampling data is increased in the correlation operation.

Additionally, the synthesized signal generator is the time base of the ADC, so its frequency stability will affect the system. The frequency stability of the HP8662A is about 2.66×10^{-12} in a 1-second interval. If we want to design a more precise system, the frequency stability of ADC's time base must be better. Figure 6 shows that the quantization error affects the measurement of the DUT accuracy. Figure 7 shows the frequency stability of the HP8662A.

EXPERIMENTAL RESULT

A self-test has been designed to verify the system resolution. The primary frequency is input to the ADC of the system. The system frequency stability is about 4.28×10^{-12} in a 1-second interval. Figure 8 shows the self-test result.

CONCLUSIONS

We have designed a high-precision counter for phase and frequency measurement, and the system resolution is about 5×10^{-12}. In our design, the idea of a software radio is used to be the main system of the counter. Despite the fact that the ADC in our system runs at about 40 MS/s, the speed of the DSP is not good enough to process all the 1-second samples. The cache memory is also not sufficient to store all the sampling data. We will solve this problem and improve the system resolution in future work. The other problem is that the ADC's time base affects the resolution of the system. The synthesized signal generator should be replaced by the mixer and the filter; furthermore, the phase noise should be lower.

ACKNOWLEDGMENTS

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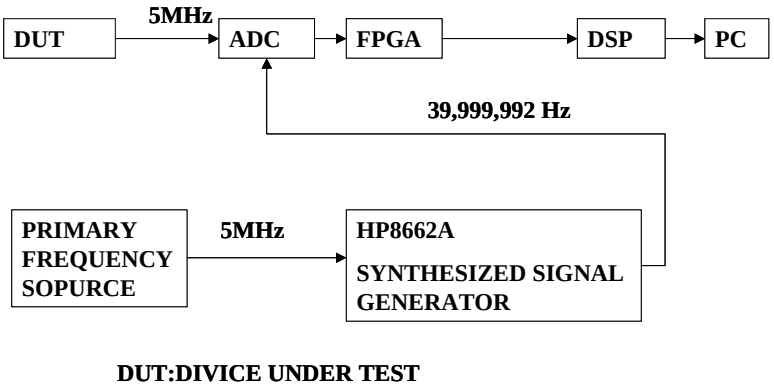
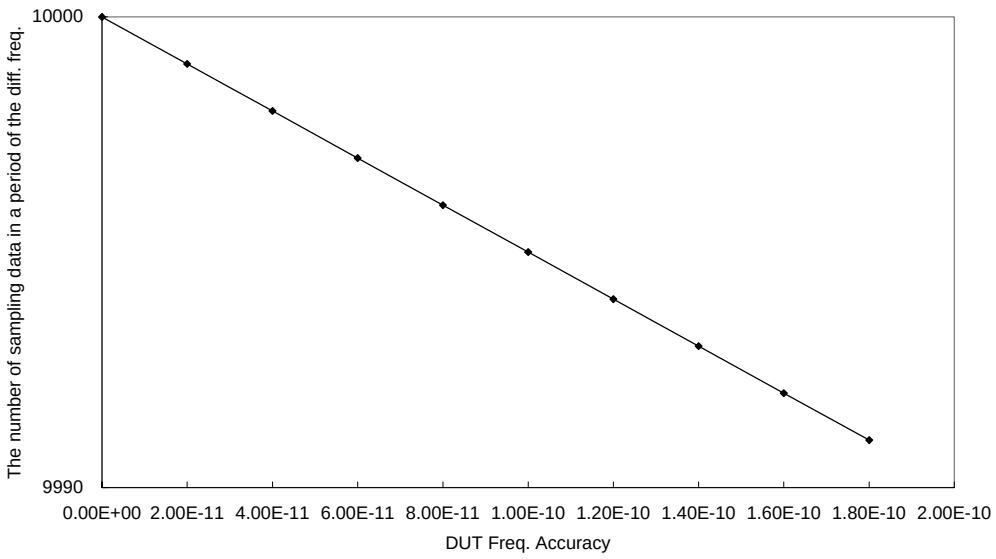


Figure 1. The block diagram for the high-precision counter.



DUT Freq.	DUT Freq. Accuracy	Sampling freq.	The diff. freq between the DUT and 500×sampling freq.	The number of sampling data in a period of the diff. freq.
5000000.0000	0.00E+00	9999.9980	1.0000	9999.9980
5000000.0001	2.00E-11	9999.9980	1.0001	9998.9981
5000000.0002	4.00E-11	9999.9980	1.0002	9997.9984
5000000.0003	6.00E-11	9999.9980	1.0003	9996.9989
5000000.0004	8.00E-11	9999.9980	1.0004	9995.9996
5000000.0005	1.00E-10	9999.9980	1.0005	9995.0005
5000000.0006	1.20E-10	9999.9980	1.0006	9994.0016
5000000.0007	1.40E-10	9999.9980	1.0007	9993.0029
5000000.0008	1.60E-10	9999.9980	1.0008	9992.0044
5000000.0009	1.80E-10	9999.9980	1.0009	9991.0061

Figure 2. The relation between the DUT accuracy and number of the sampling data in a period of the difference frequency.

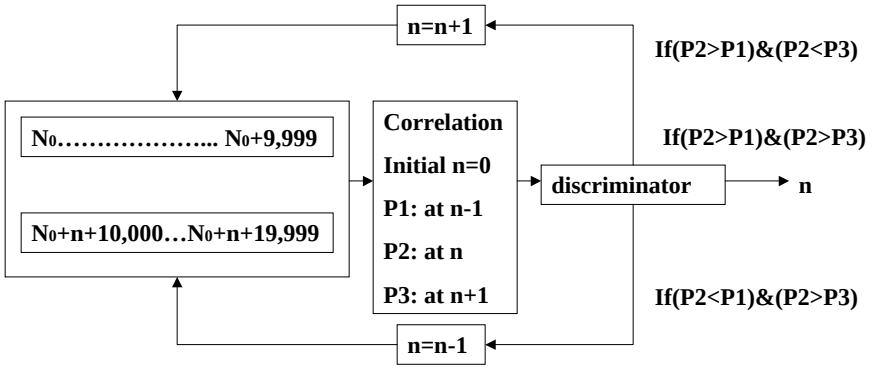


Figure 3. The correlation operation.

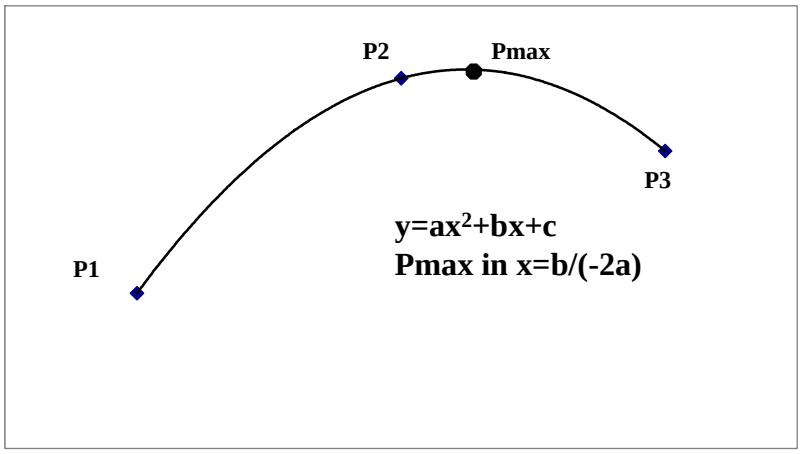


Figure 4. The floating part of the sampling number is determined by the quadratic fit.

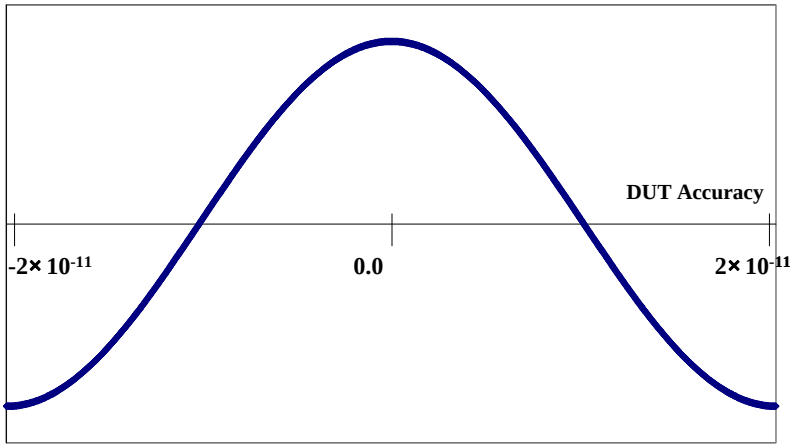


Figure 5. Correction result is mapped to the DUT accuracy.

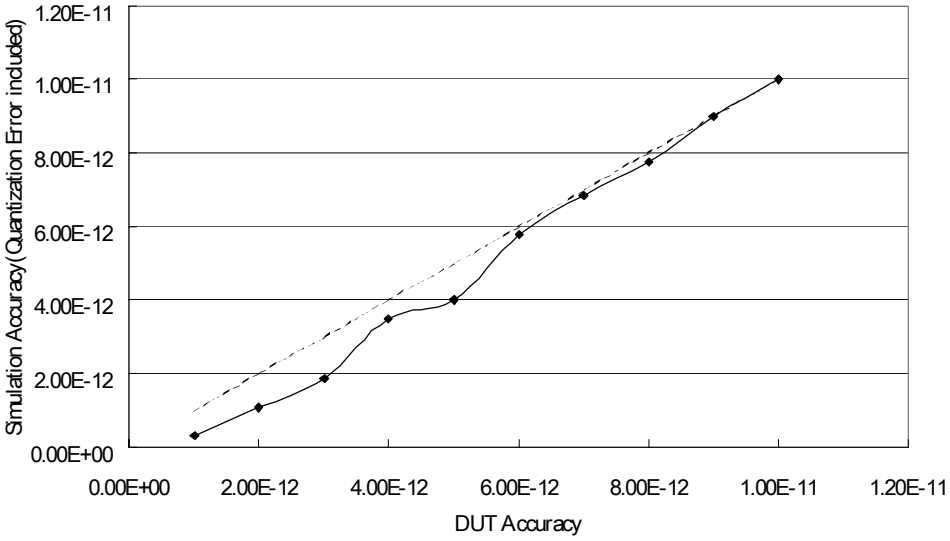


Figure 6. The quantization error affects the system resolution.

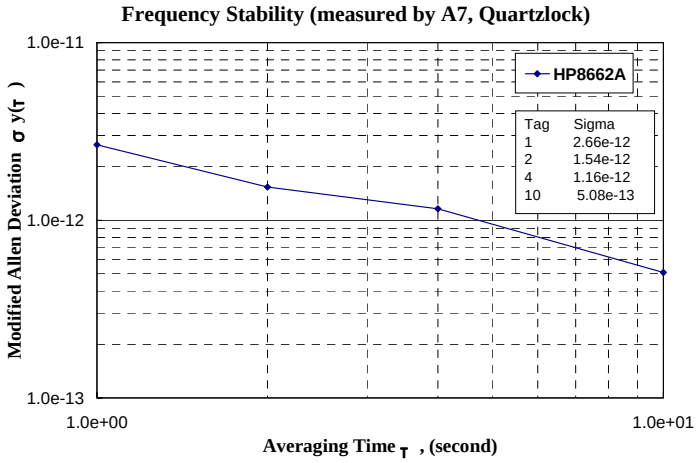


Figure 7. The time base error of the ADC.

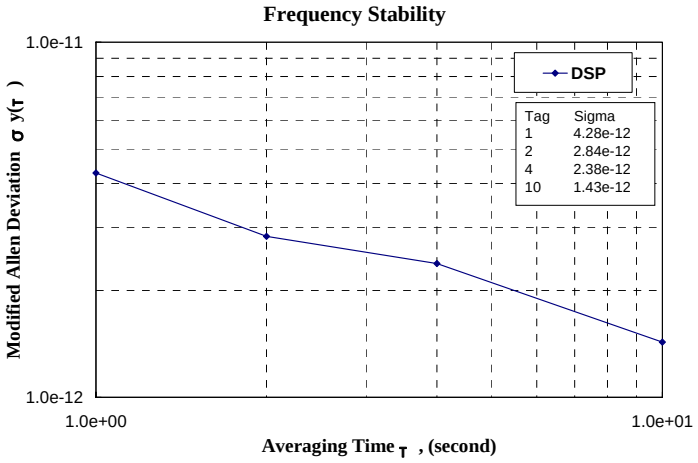


Figure 8. The self-test frequency stability.